DESCRIPTION

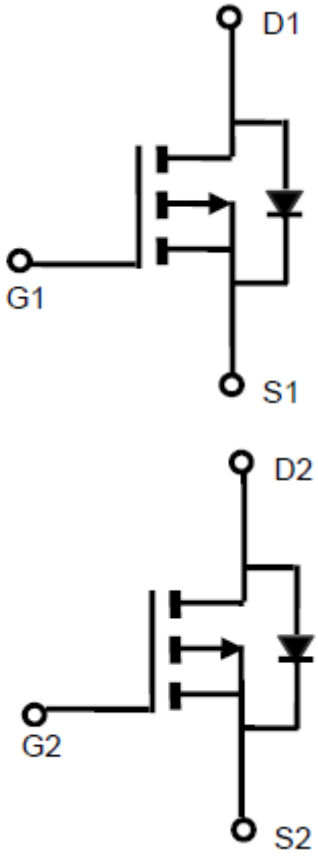
The MP4953 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

This MP4953 is particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

The MP4953 is available in SOP8 Package

P-CHANNEL MOSFET



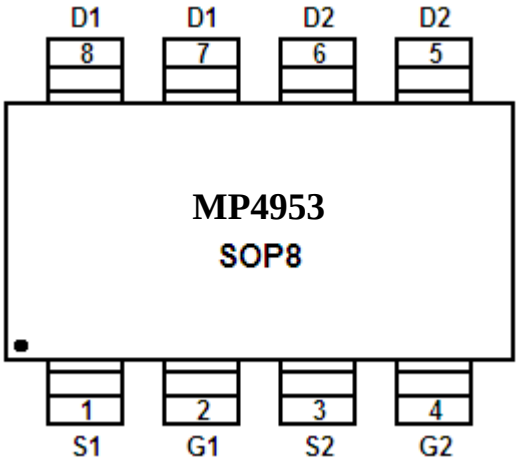
FEATURES

- -30V/-5.2A, $R_{DS(ON)}$ < 60mΩ@V_{GS} = -10V
- -30V/-4.5A, $R_{DS(ON)}$ < 90mΩ@V_{GS} = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- Available in SOP8 package

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN DESCRIPTION



Top View

Pin #	Symbol	Function
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

ABSOLUTE MAXIMUM RATINGS

T_A = 25℃ Unless otherwise specified

Drain-Source Voltage (V_{DSS})		-30V
Gate-Source Voltage (V_{GSS})		±20V
Continuous Drain Current (T_J=150℃) (V_{GS}=-10V) (I_D)		-5.2A
Pulsed Drain Current (I_{DM})		-20A
Continuous Source Current (Diode Conduction) (I_S)		-2.4A
Operation Junction Temperature (T_J)		-55℃ ~ 150℃
Storage Temperature Range (T_{STG})		-55℃ ~ 150℃
Power Dissipation (P_D)	T_A =25℃	2.8W
	T_A =70℃	1.8W
Thermal Resistance-Junction to Ambient ($R_{\theta JA}$)		70℃/W

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

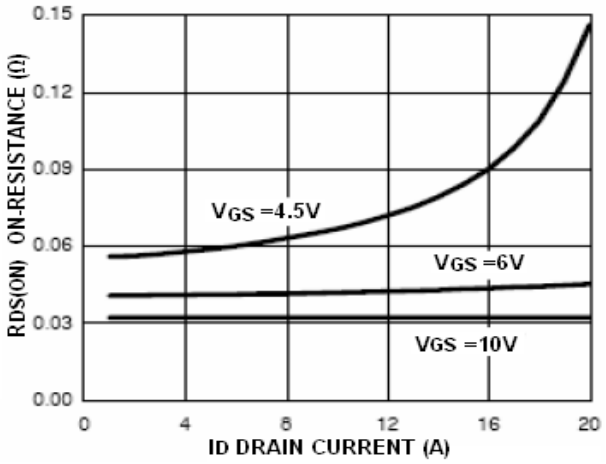
T_A = 25℃ Unless otherwise specified.

Parameter	Symbol	Conditions	Min	Type	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} =0V,I_D =-250μA	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS},I_D =-250μA	-1.0	-	-3.0	V
Gate Leakage Current	I_{GSS}	V_{DS} =0V,V_{GS}=±20V	-	-	±100	nA
Zero GATE Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V	-	-	-1	μA
		V_{DS}=-30V,V_{GS}=0V,T_J=55℃	-	-	-5	
On-State Drain Current	$I_{D(ON)}$	V_{DS} ≦-5V,V_{GS} ≦-10V	-25	-	-	A
Drain-source On-Resistance	$R_{DS(ON)}$	V_{GS} =-10V,I_D=-5.2A	-	45	60	mΩ
		V_{GS} =-4.5V, I_D=-4.5A		60	90	
Forward Tran conductance	G_{fs}	V_{DS} =-10V,I_D=-5.2A	-	10	-	S
Diode forward Current (Max.)	I_S	-	-	-	2.6	A
Diode Forward Voltage	V_{SD}	I_S=-2.0A,V_{GS}=0V	-	-0.8	-1.2	V
Total Gate Charge	Q_G	V_{DS} =-15V,V_{GS} =-10V I_D =-5.0A	-	15	10	nC
Gate-Source Charge	Q_{GS}		-	4.0	-	
Gate-Drain Charge	Q_{GD}		-	2.0	-	
Input Capacitance	C_{iss}	V_{DS} =-15V,V_{GS} =0V f =1MHz	-	680	-	pF
Output Capacitance	C_{oss}		-	120	-	
Reverse Transfer Capacitance	C_{rss}		-	75	-	
Turn-On Time	td(on)	V_{DD} =-15V,R_L =15Ω I_D =-1.0A,V_{GEN} =-10V R_G =6Ω	-	7.0	15	nS
	tr		-	10	20	
Turn-Off Time	td(off)		-	40	80	
	tf		-	20	40	

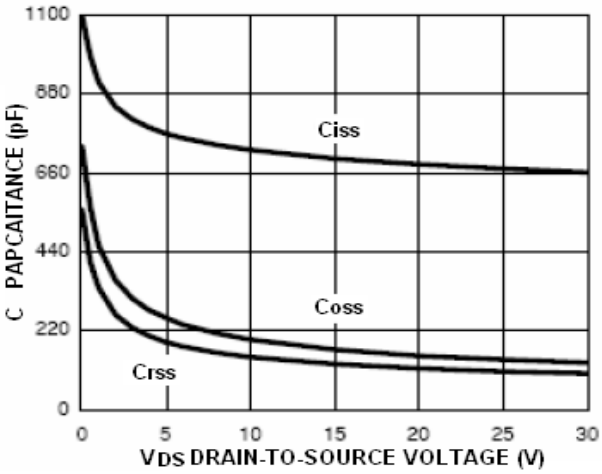
Note : 1. Pulse test: pulse width <= 300us, duty cycle<= 2%
2. Static parameters are based on package level with recommended wire-bonding

TYPICAL PERFORMANCE CHARACTERISTICS

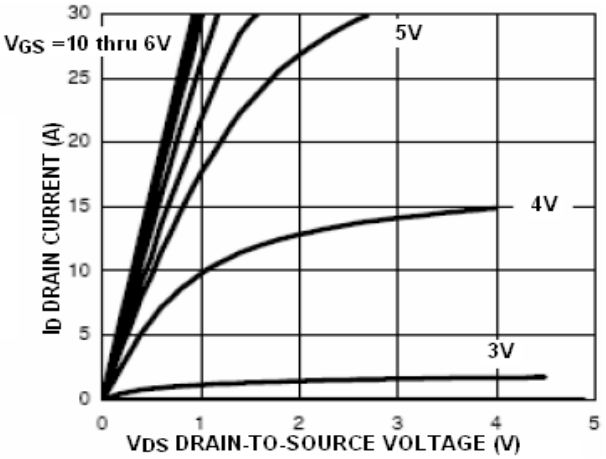
1. ON-Resistance vs. Drain Current



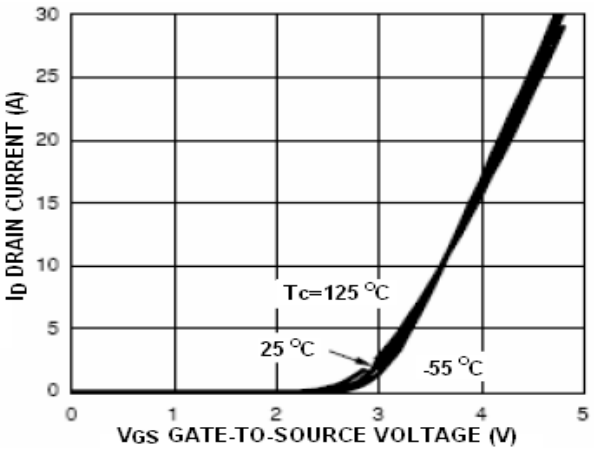
2. Capacitance



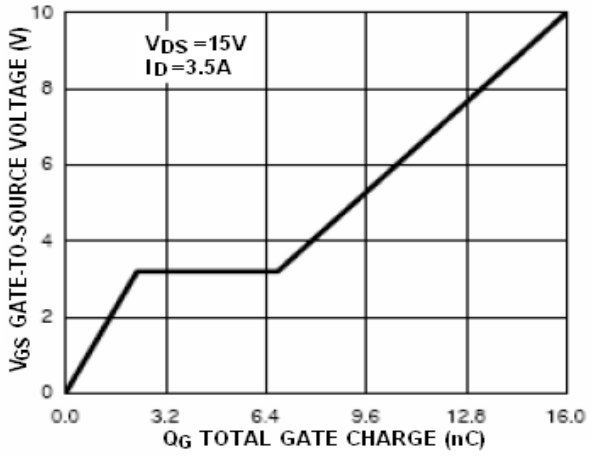
3. Output Characteristics



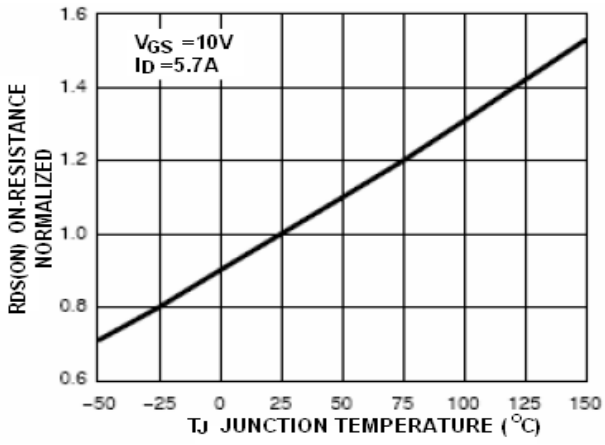
4. Transfer Characteristics



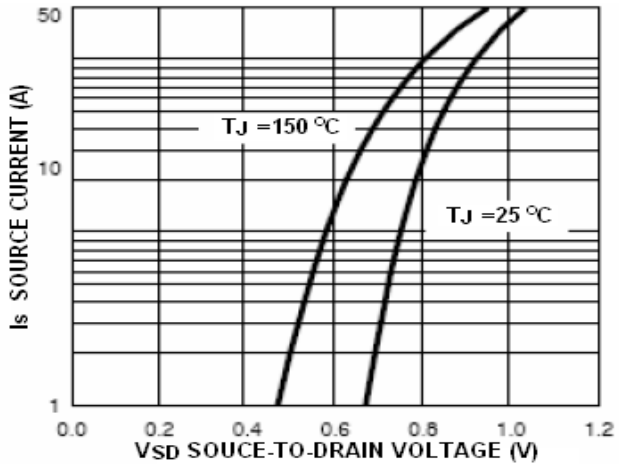
5. Gate Charge



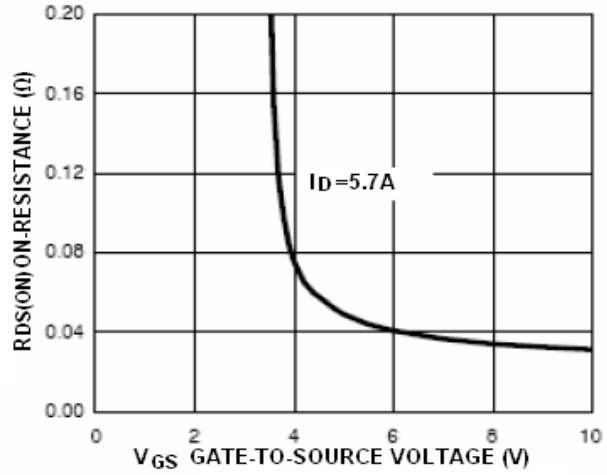
6. On-Resistance vs. Junction Temperature



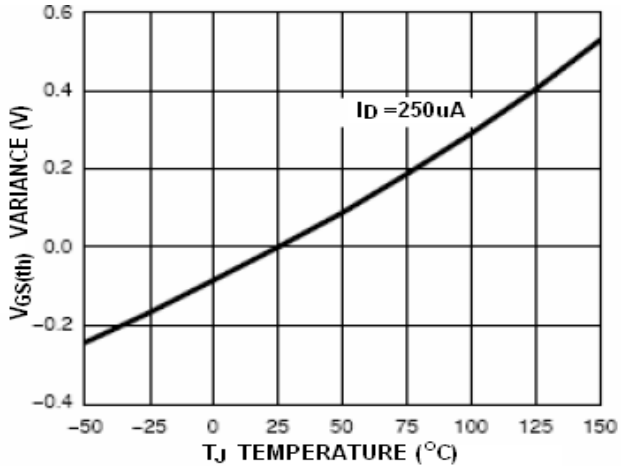
7. Source Drain Diode Forward Voltage



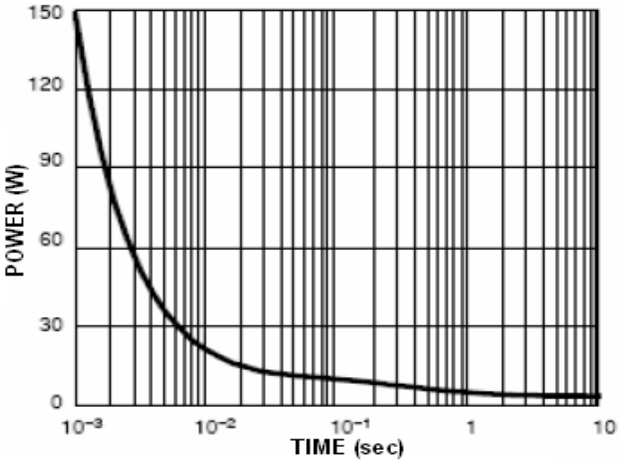
8. On-Resistance vs. Gate-to-Source Voltage



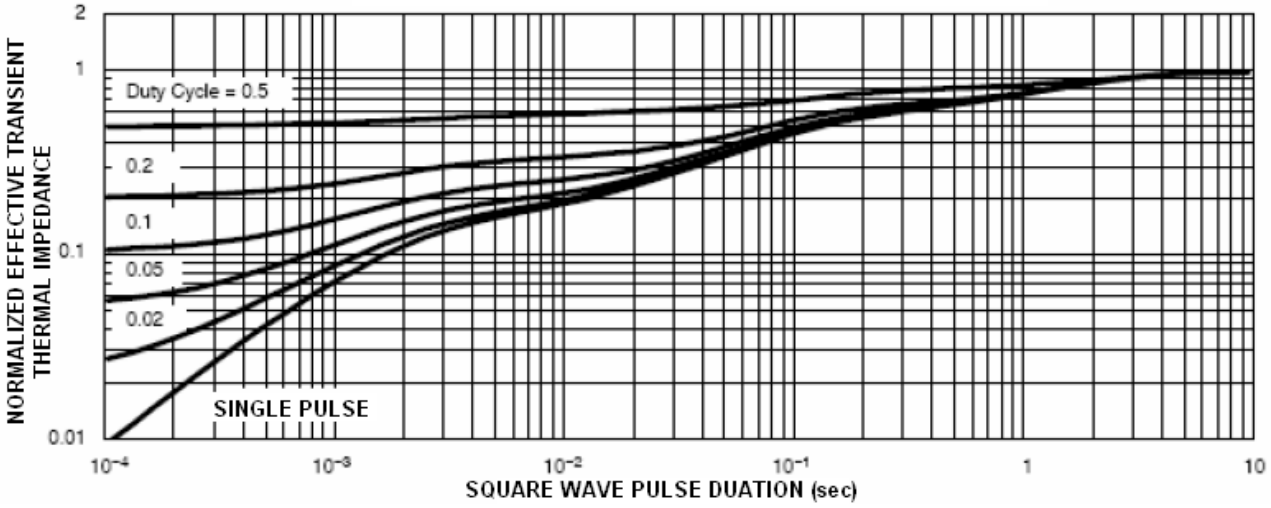
9. Threshold Voltage



10. Single Pulse Power, Junction-to-Ambient

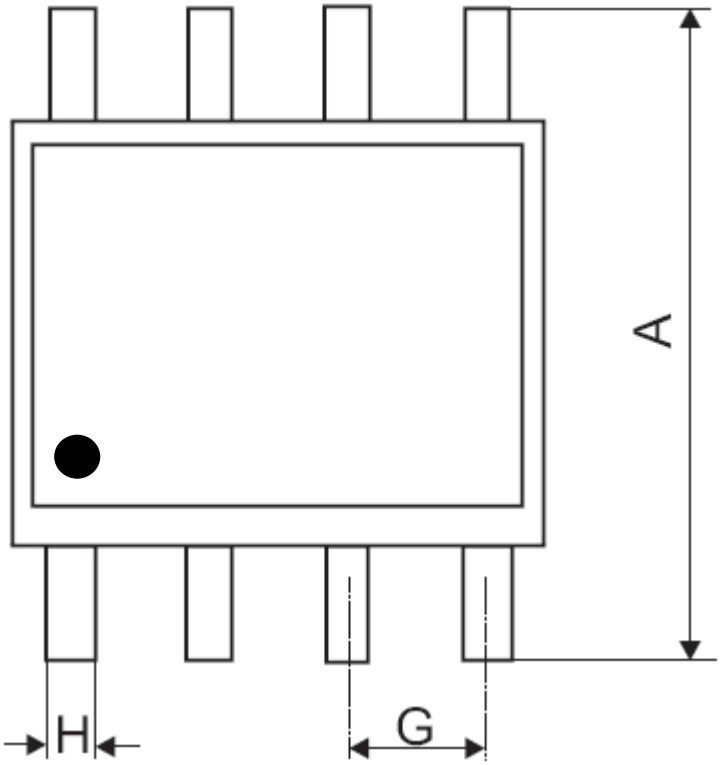


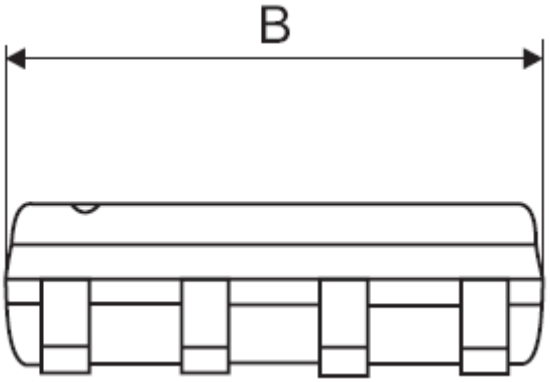
11. Normalized Thermal Transient Impedance, Junction-to-Foot

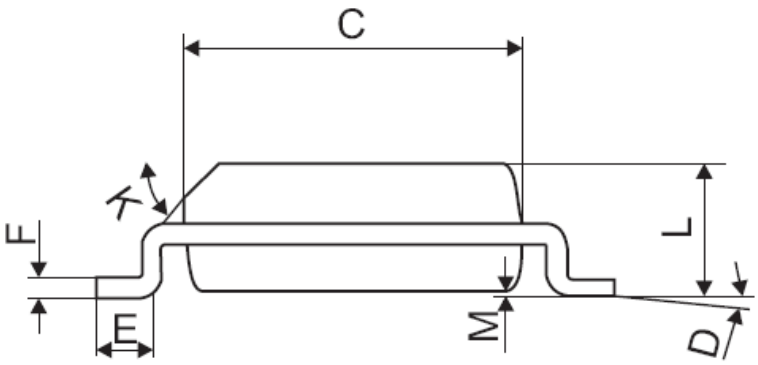


PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)







Symbol	Min	Nom	Max
A	5.80	6.00	6.20
B	4.80	4.90	5.00
C	3.80	3.90	4.00
D	0	4	8
E	0.40	0.65	0.90
F	0.19	0.22	0.25
G	1.27TYP		
H	0.35	0.42	0.49
J	0.375REF		
K	45		
L	1.35	1.55	1.75
M	0	0.07	0.15