Major Power Technology Co.,Ltd.

MP72X High Sensitivity Hall Latch

Revision 0.2

2009/06/05

1. Overview

Features

☐**Wide Operating Voltage Range:**
-Single supply voltage 3.5-24V
☐**Specified Operating Temperature Range:**
-From –40C up to 125C
☐**High Magnetic Sensitivity**
☐**Chopper-Stabilized Amplifier Stage**
☐**Lower Power Consumption**
☐**Open Drain Output**
☐**High ESD Capability**
-4KV HBM ESD Capability

Application Examples

☐**Automotive, Consumer and Industrial**
☐**Solid-State Switch**
☐**Brushless DC Motor Commutation**
☐**Speed Detection**
☐**Linear Position Detection**
☐**Angular Position Detection**
☐**Proximity Detection**

Product Description

The MP72X is a Hall-effect latch designed in mixed-signal CMOS technology. The device integrates a voltage regulator, Hall sensor with dynamic offset cancellation system, Schmitt trigger and an open-drain output driver, all in a single package.

Thanks to its wide operating voltage range and extended choice of temperature range, it is quite suitable for use in automotive, industrial and consumer applications.

The device is delivered in a Thin Small Outline Transistor (TSOT) for surface mount process and in a Plastic Single In Line (TO-92 flat) for through hole mount.

Both 3-lead packages are RoHS compliant.

Pin Configuration

Table 1-1: Pin definition and description for TSOT-3L

No	Pin	Function
1	VDD	Power
2	OUT	Open Drain Output
3	GND	Ground

Table 1-2: Pin definition and description for TO92 flat

No	Pin	Function
1	VDD	Power
2	GND	Ground
3	OUT	Open Drain Output

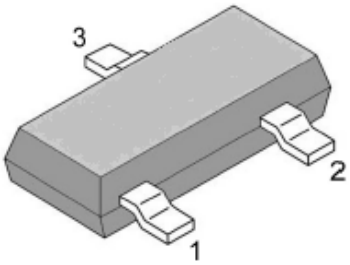


Figure 1-1 TSOT23 package

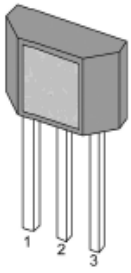


Figure 1-2 Flat TO92 flat package

2. General

2.1 Brief Theory of Operation

-The magnetic flux is transferred to voltage signal by the Hall device.
-The Instrument amplifier amplifies the Hall voltage into a large swing signal.
- The dynamic offset cancelation system reduce the offset of Hall device and amplifier
-The hysteresis comparator converts the amplified signal into switch signal as to the setting
-The output stage latches the comparator out, and gives a open drain output

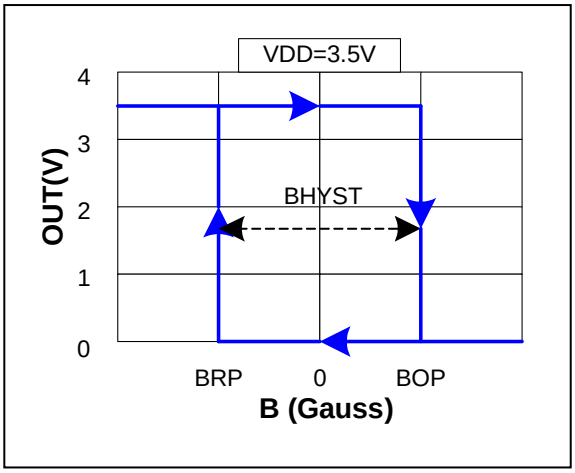


Figure 2-1: Example of Sensor Output

2.2 Transfer Function

Figure 2-1 shows one transfer example of the device.

2.3 Block Diagram

Figure 2-2 shows the simplified block structure.

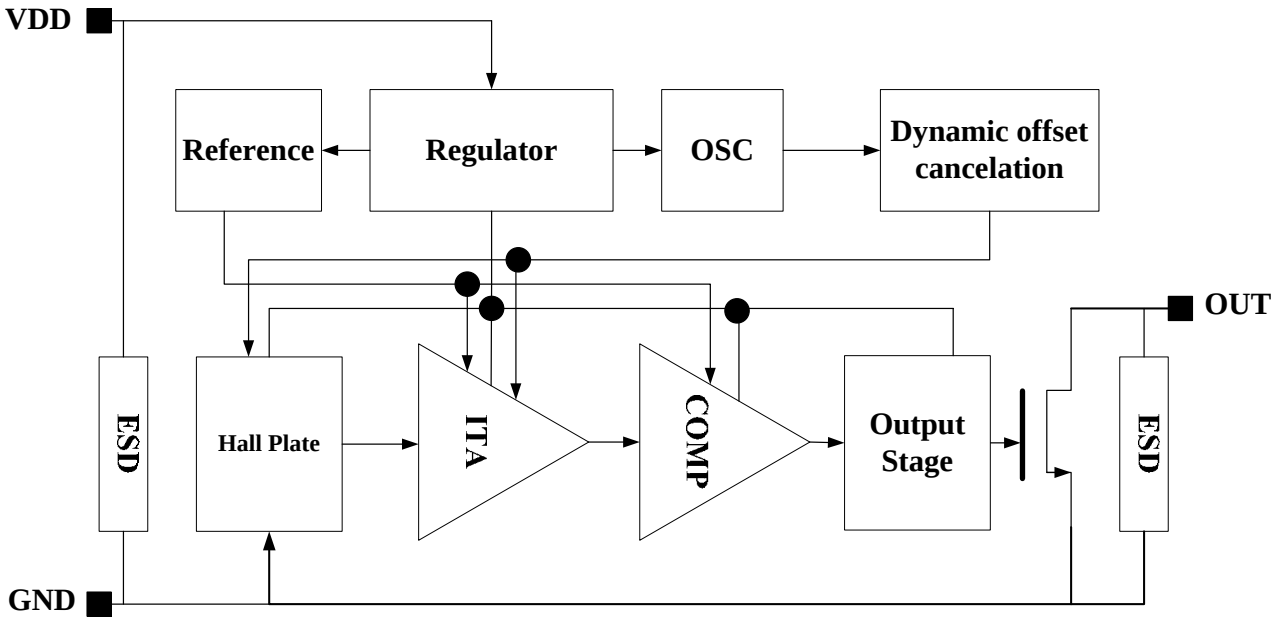


Figure 2-2: Block Diagram

3. Function Description

3.1 Definition of Magnetic Parameters

BOP: Operating Point
Magnetic flux density applied on the branded side of the package which turns the output driver ON (V_{OUT} = V_{DSon})

BRP: Release Point
Magnetic flux density applied on the branded side of the package which turns the output driver OFF (V_{OUT} = high)

BHYST: Hysteresis Window
BOP-BRP

3.2 Definition of Switching Function

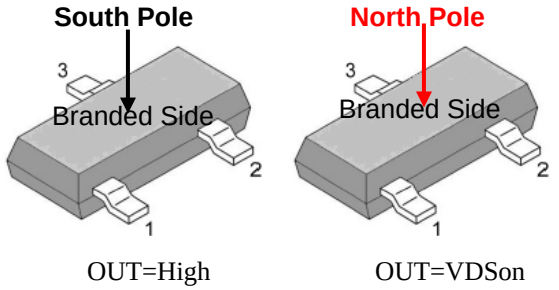


Figure 3-1: Switching Point of TSOT23

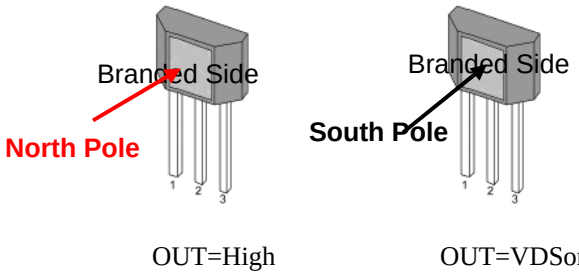


Figure 3-2: Switching Point of TO92 Flat

DC Operating Parameters TA = -40C to 125C, VDD = 3.5V to 24V (unless otherwise specified)

Table 3-1: Switching Function

Parameter	Pole(TSOT23)	OUT(TSOT23)	Pole(TO92 Flat)	OUT(TO92 Flat)
South Pole	B<BRP	High	B>BOP	VDSon
North Pole	B>BOP	VDSon	B<BRP	High

3.3 Latch Characteristic

The device exhibits latch magnetic switching characteristics. Therefore, it requires both south and north poles to operate properly.

The device behaves as a latch with symmetric operating and release switching points (B_{OP}=|B_{RP}|). This means magnetic fields with equivalent strength and opposite direction drive the output high and low. Removing the magnetic field (B→0) keeps the output in its previous state. This latching property defines the device as a magnetic memory.

A magnetic hysteresis B_{HYST} keeps B_{OP} and B_{RP} separated by a minimal value. This hysteresis prevents output oscillation near the switching point.

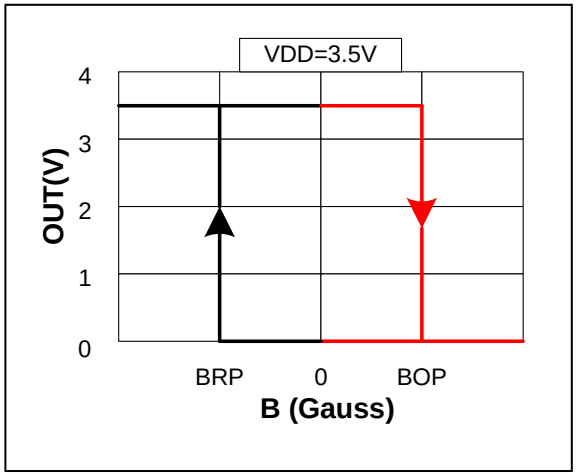


Figure 3-3: Latch Characteristic
TSOT23 Package

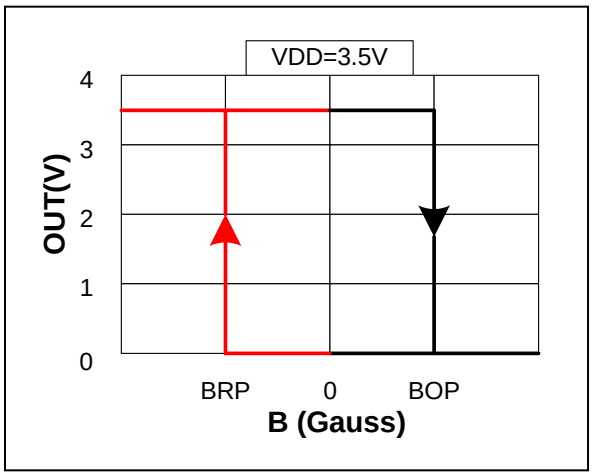


Figure 3-4: Latch Characteristic
TO92 Flat Package

Note:

South Pole
North Pole

4. Electrical and Magnetic Characteristics

4.1 Absolute Maximum Ratings

Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

Table 4-1: Absolute maximum ratings: all voltages listed are referenced to GND

Symbol	Parameters	Min	MAX	Unit	Notes
Ts	Storage temperature	-50	150	C	
T_J	Junction temperature	-50	150	C	
VDD	Supply voltage		28	V	
IDD	Supply current		50	mA	
V_{OUT}	Output voltage		28	V	
I_{OUT}	Continuous output current		50	mA	

4.2 Electrical Characteristics

Table 4-2: Characteristics: at T_a=-40C to +125C, VDD=3.5 to 24V, if not otherwise specified.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage	V_{DD}	Operating	3.5		24	V
Supply Current	I_{DD}	B< B_{RP}			5	mA
Output Saturation Voltage	V_{DSON}	I_{OUT} = 20mA, B > B_{OP}			0.5	V
Output Leakage Current	I_{OFF}	B< B_{RP}, V_{OUT}=24V			10	uA
Output Rise Time	T_R	R_L=1KOhm, C_L=20pF			0.45	uS
Output Fall Time	T_F	R_L=1KOhm, C_L=20pF			0.45	uS
Maximum Switching Frequency	F_{SW}			10		KHz
Package Thermal Resistance	R_{TH}	Single layer (1S) Jedec board		301		° C/W
Magnetic Operating Point	B_{OP}		0.5		5.0	mT
Magnetic Release Point	B_{RP}		-5.0		-0.5	mT
Hysteresis Window	B_{HYST}		5.6	8	10.4	mT
Electro-Static Discharge	ESD	HBM		4		KV

4.3 Typical Characteristics

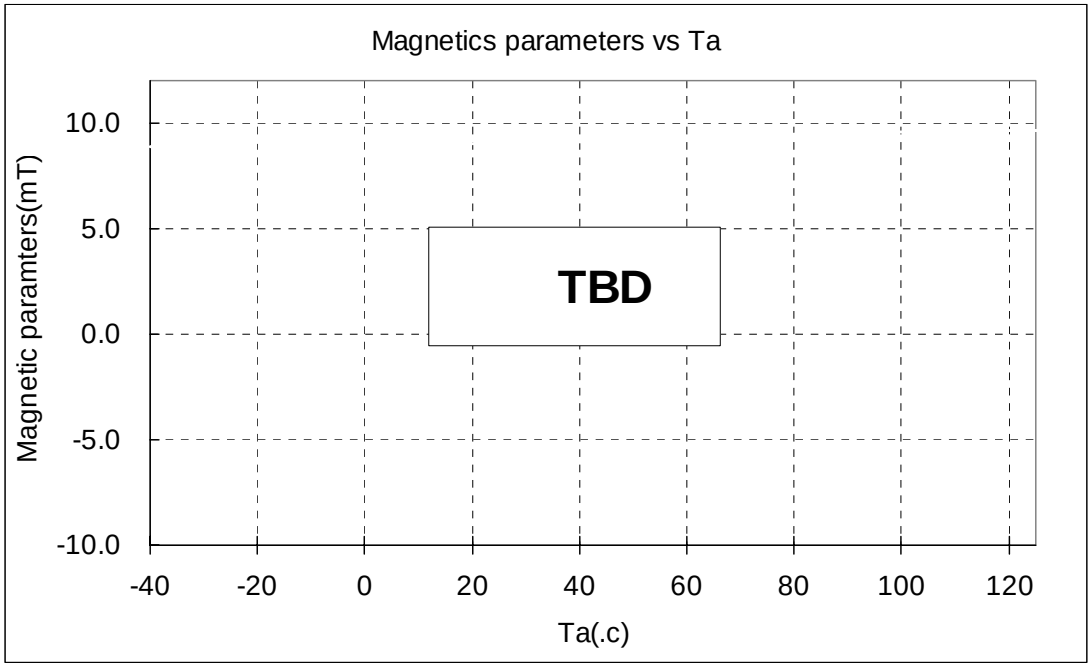


Figure 4-1: Magnetic parameters VS Ta

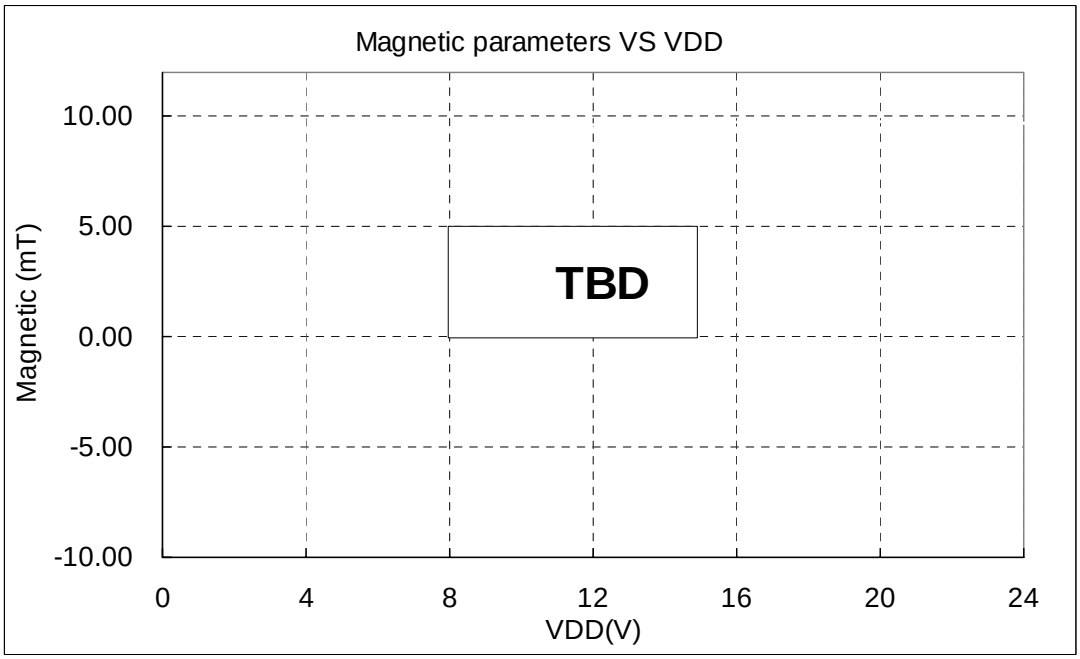


Figure 4-2: Magnetic parameters VS VDD

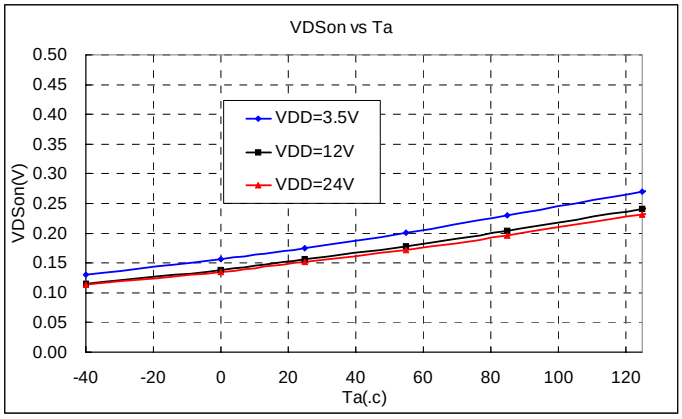


Figure 4-3: VDSon VS Ta

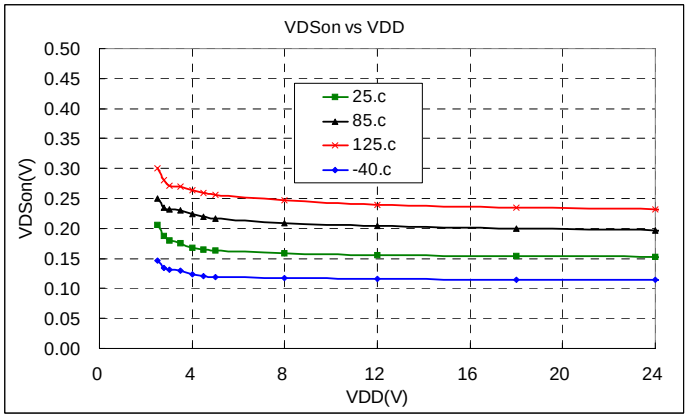


Figure 4-4: VDSon VS VDD

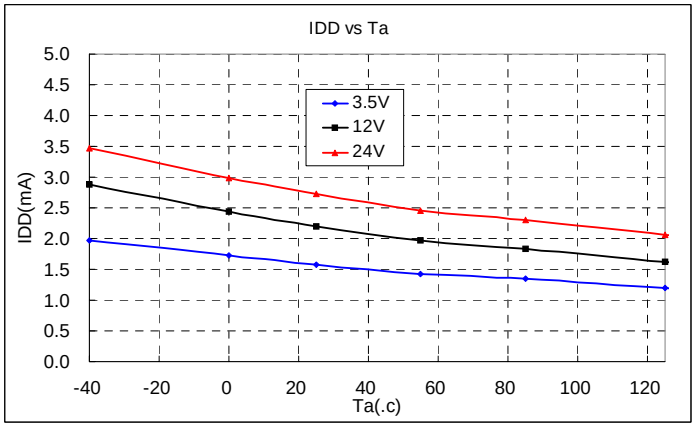


Figure 4-5: IDD VS Ta

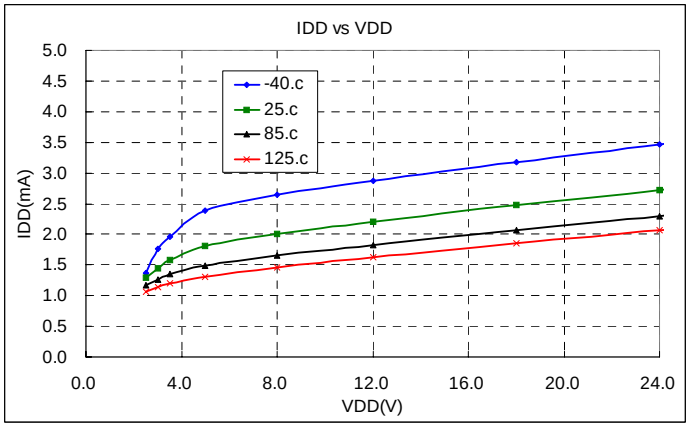


Figure 4-6: IDD VS VDD

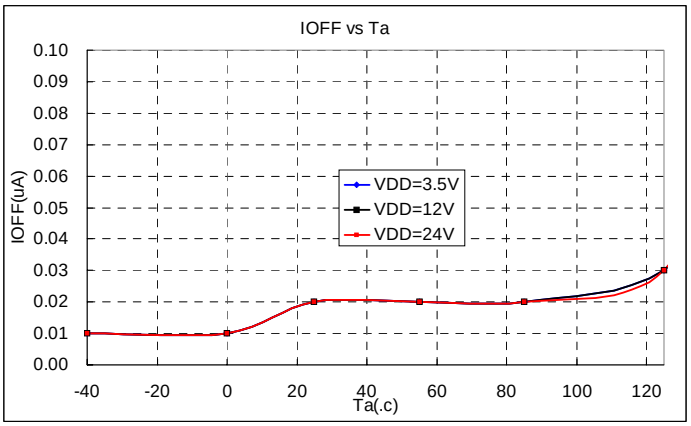


Figure 4-7: IOFF VS Ta

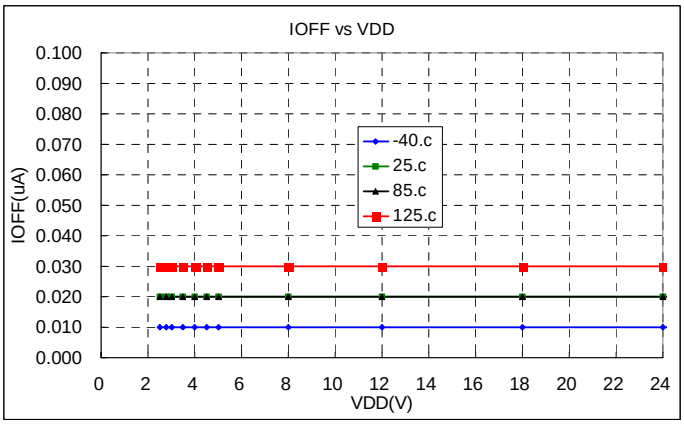
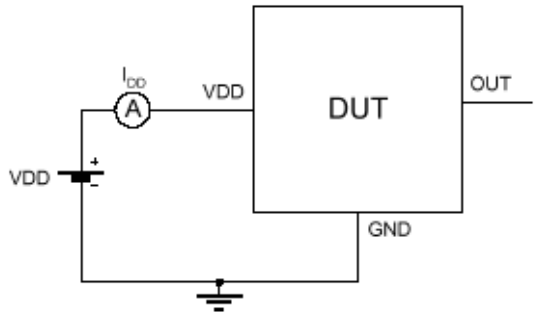


Figure 4-8: IOFF VS VDD

4.4 Test Conditions

Note: DUT= Device Under Test

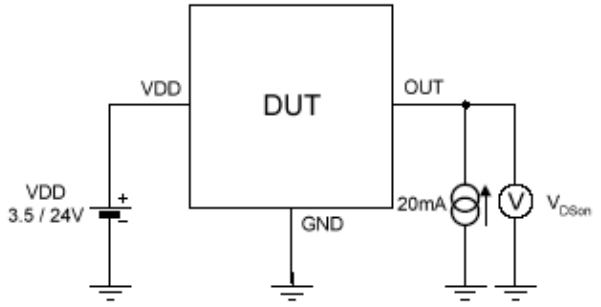
Supply Current



Note1- The supply current IDD represents the static supply current. Out is left open when measurement
Note2- The device is put under magnetic field with B<BRP

Figure 4-9: IDD Test Condition

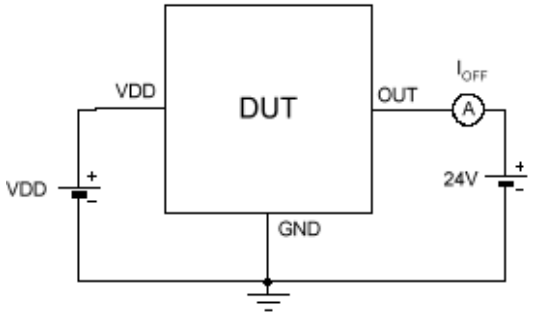
Output Saturation Voltage



Note1- The output saturation voltage VDSon is measured at Vdd=3.5V and VDson=24V.
Note2- The device is put under magnetic field with B>BOP

Figure 4-10: VDSon Test Condition

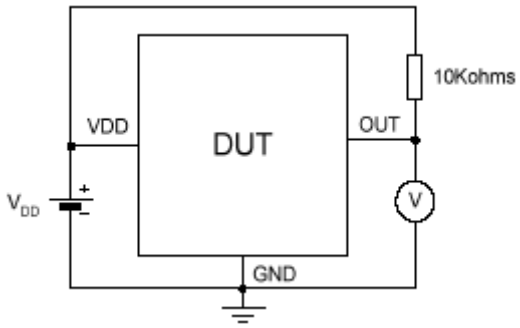
Output Leakage Current



Note1- The device is put under magnetic field with B<BRP

Figure 4-11: IOFF Test Condition

Magnetic Thresholds



Note1- BOP is determined by putting the device under magnetic field swept from BRPmin up to BOPmax until the output is switch on
Note2- BRP is determined by putting the device under magnetic field swept from BOPmax down to BRPmin until the output is switch off

Figure 4-12: Magnetic parameters Test Condition

5. Application Information

4.1 Typical Three –Wire Application Circuit

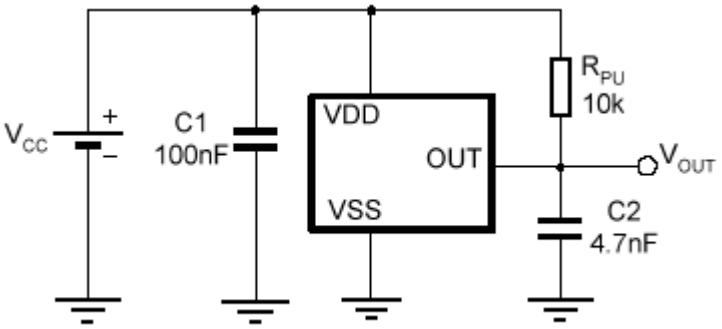


Figure 5-1: 3-Wire Application Circuit

4.2 Two-Wire Application Circuit

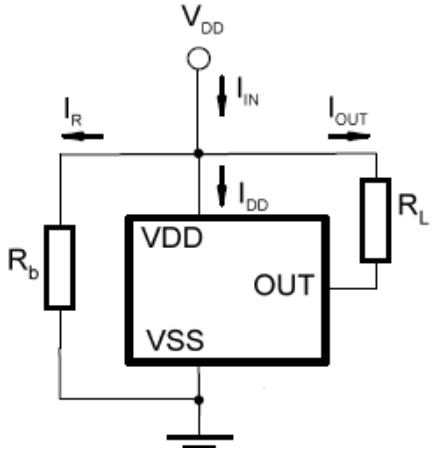


Figure 5-2: 2-Wire Application Circuit

Note:
With this circuit, precise ON and OFF currents can be detected using only two connecting wires.
The resistors RL and Rb can be used to bias the input current. Refer to the part specifications for limiting values.
BRP: IOFF = IR + IDD = VDD/Rb + IDD
BOP: ION = IOFF + IOUT = IOFF + VDD/RL
Because the IOUT has the limitation, Please select the resistance of Rb and RL carefully for this application

4.3 Three-Wire Circuit For Automotive and Harsh, Noisy Application

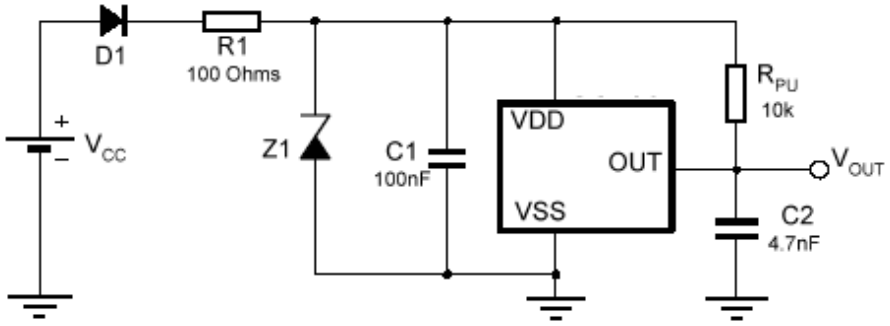


Figure 5-3: 3-Wire Application Circuit For Harsh and Noisy Environment

4.4 Application Comments

4.4.1 For proper operation, a 100nF bypass capacitor should be placed as close as possible to the device between the VDD and ground pin.

4.4.2 For reverse voltage protection, it is recommended to connect a resistor or a diode in series with the VDD pin. When using a resistor, three points are important:

- The resistor has to limit the reverse current to 50mA maximum (VCC / R1 ≤ 50mA)
- The resulting device supply voltage VDD has to be higher than VDD min (VDD = VCC – R1×IDD)
- The resistor has to withstand the power dissipated in reverse voltage condition (PD = VCC^2 / R1)

When using a diode, a reverse current cannot flow and the voltage drop is almost constant(≈0.7V). Therefore, a 100W/0.25W resistor for 5V application and a diode for higher supply voltage are recommended. Both solutions provide the required reverse voltage protection.

4.4.3 When a weak power supply is used or when the device is intended to be used in noisy environment, it is recommended that figure 13.3 from the Application Information section is used. The low-pass filter formed by R1 and C1 and the Zener diode Z1 bypass the disturbances or voltage spikes occurring on the device supply voltage VDD. The diode D1 provides additional reverse voltage protection.